IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of HOLGER THIEL ET AL

Atty. Docket PHDE 010015

Serial No.:

Filed: CONCURRENTLY

Title: CIRCUIT ARRANGEMENT

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

4. (Amended) A circuit arrangement as claimed in claim 2, characterized in that the first temporal delays (Δt_1) generated in the first delay unit (24) and/or the second temporal delays (Δt_2) generated in the second delay unit (34) can each be built up with gate delay times.

5. (Amended) A circuit arrangement as claimed in claim 1 , characterized in that the second modulation signal (M_2) is temporally shifted with respect to the first modulation

signal (M_1) by approximately half a clock period of the external clock signal (C_0).

6. (Amended) A circuit arrangement as claimed in claim 1, characterized in that

- the first driver stage (40) comprises:
  - a clock signal input (42c) provided for the first clock signal (C_1);
  - a modulation signal input (42m) provided for the first modulation signal (M_1) for controlling the switching of each modulation voltage (U_unmod or U_mod) to the amplitude-modulated first power supply voltage ($U_{dd,1}$);
  - a first electronic switch (44);
  - a second electronic switch (46) arranged behind the first switch (44); and
  - an output (48) provided for the first output signal comprising the output voltage ($U_{o,1}$),
    - wherein the control means (442) of the first switch (44) and the control means (462) of the second switch (46) are each connected to the clock signal input (42c);
    - the power supply voltage-sided contact (444) of the first switch (44) is connected to the amplitude-modulated first power supply voltage ($U_{dd,1}$),

- the reference potential-sided contact (464) of the second switch (46) is connected to the first reference potential ($U_{ss,1}$), and
- the output voltage-sided contact (446) of the first switch (44) and the output voltage-sided contact (466) of the second switch (46) are connected together and to the output (48), and

- in that the second driver stage (50) comprises:
  - a clock signal input (52c) provided for the second clock signal (C_2);
  - a modulation signal input (52m) provided for the second modulation signal (M_2) for controlling the switching of each modulation voltage (U_unmod or U_mod) to the amplitude-modulated second power supply voltage ($U_{dd,2}$);
  - a first electronic switch (54);
  - a second electronic switch (56) arranged behind the first switch (54); and
  - an output (58) provided for the second output signal comprising the output voltage ($U_{o,2}$),
    - wherein the control means (542) of the first switch (54) and the control means (562) of the second switch (56) are each connected to the clock signal input (52c),
    - the power supply voltage-sided contact (544) of the first switch (54) is connected to the

amplitude-modulated second power supply voltage ($U_{dd,2}$),

- the reference potential-sided contact (564) of the second switch (56) is connected to the second reference potential ($U_{ss,2}$), and
- the output voltage-sided contact (546) of the first switch (54) and the output voltage-sided contact (566) of the second switch (56) are connected together and to the output (58).

8. (Amended) A circuit arrangement as claimed in claim 1, characterized in that the first driver stage (40) and the second driver stage (50) are complementary with respect to each other.

9. (Amended) A circuit arrangement as claimed in claim 1, characterized in that the first power supply voltage ($U_{dd,1}$) and the second power supply voltage ($U_{dd,2}$) have different values.

10. (Amended) A circuit arrangement as claimed in claim 1, characterized in that the first reference potential ($U_{ss,1}$) and the second reference potential ($U_{ss,2}$) are at least approximately equally large.

11. (Amended) A circuit arrangement as claimed in claim 1, characterized in that the first reference potential ($U_{ss,1}$) and/or the second reference potential ($U_{ss,2}$) are the earth potential or the ground potential.

12. (Amended) A preferably contactless integrated circuit, particularly a CMOS circuit controlled and particularly tested by at least a circuit arrangement (100) as claimed in claim 1.

REMARKS

The foregoing Preliminary Amendment to claims 4-6, and 8-12 was made solely to avoid filing the claims in the multiple dependant form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights she may have under the Doctrine of Equivalents. Applicant furthermore reserves her right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

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APPENDIX

4. (Amended) A circuit arrangement as claimed in claim 2 ~~or 3~~, characterized in that the first temporal delays (Δt_1) generated in the first delay unit (24) and/or the second temporal delays (Δt_2) generated in the second delay unit (34) can each be built up with gate delay times.

5. (Amended) A circuit arrangement as claimed in ~~any one of~~ claim~~s~~ 1 ~~to 4~~, characterized in that the second modulation signal (M_2) is temporally shifted with respect to the first modulation signal (M_1) by approximately half a clock period of the external clock signal (C_0).

6. (Amended) A circuit arrangement as claimed in ~~any one of~~ claim~~s~~ 1 ~~to 5~~, characterized in that

- the first driver stage (40) comprises:
  - a clock signal input (42c) provided for the first clock signal (C_1);
  - a modulation signal input (42m) provided for the first modulation signal (M_1) for controlling the switching of each modulation voltage (U_unmod or U_mod) to the amplitude-modulated first power supply voltage ($U_{dd,1}$);
  - a first electronic switch (44);

- a second electronic switch (46) arranged behind the first switch (44); and
- an output (48) provided for the first output signal comprising the output voltage ($U_{o,1}$),
  - wherein the control means (442) of the first switch (44) and the control means (462) of the second switch (46) are each connected to the clock signal input (42c);
  - the power supply voltage-sided contact (444) of the first switch (44) is connected to the amplitude-modulated first power supply voltage ($U_{dd,1}$),
  - the reference potential-sided contact (464) of the second switch (46) is connected to the first reference potential ($U_{ss,1}$), and
  - the output voltage-sided contact (446) of the first switch (44) and the output voltage-sided contact (466) of the second switch (46) are connected together and to the output (48), and

- in that the second driver stage (50) comprises:
  - a clock signal input (52c) provided for the second clock signal (C_2);
  - a modulation signal input (52m) provided for the second modulation signal (M_2) for controlling the switching of each modulation voltage (U_unmod or

U_mod) to the amplitude-modulated second power supply voltage ($U_{dd,2}$);

- a first electronic switch (54);
- a second electronic switch (56) arranged behind the first switch (54); and
- an output (58) provided for the second output signal comprising the output voltage ($U_{o,2}$),
  - wherein the control means (542) of the first switch (54) and the control means (562) of the second switch (56) are each connected to the clock signal input (52c),
  - the power supply voltage-sided contact (544) of the first switch (54) is connected to the amplitude-modulated second power supply voltage ($U_{dd,2}$),
  - the reference potential-sided contact (564) of the second switch (56) is connected to the second reference potential ($U_{ss,2}$), and
  - the output voltage-sided contact (546) of the first switch (54) and the output voltage-sided contact (566) of the second switch (56) are connected together and to the output (58).

8. (Amended) A circuit arrangement as claimed in ~~any one of~~ claim~~s~~ 1 ~~to 7~~, characterized in that the first driver stage (40) and the second driver stage (50) are complementary with respect to each other.

9. (Amended) A circuit arrangement as claimed in ~~any one of~~ claim~~s~~ 1 ~~to 8~~, characterized in that the first power supply voltage ($U_{dd,1}$) and the second power supply voltage ($U_{dd,2}$) have different values.

10. (Amended) A circuit arrangement as claimed in ~~any one of~~ claim~~s~~ 1 ~~to 9~~, characterized in that the first reference potential ($U_{ss,1}$) and the second reference potential ($U_{ss,2}$) are at least approximately equally large.

11. (Amended) A circuit arrangement as claimed in ~~any one of~~ claim~~s~~ 1 ~~to 10~~, characterized in that the first reference potential ($U_{ss,1}$) and/or the second reference potential ($U_{ss,2}$) are the earth potential or the ground potential.

12. (Amended) A preferably contactless integrated circuit, particularly a CMOS circuit controlled and particularly tested by at least a circuit arrangement (100) as claimed in ~~any one of~~ claim~~s~~ 1 ~~to 11~~.